Blakely, Sokoloff, Taylor & Zafman LLP (310) 207-3800 Title: PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED JUNCTION REGIONS

1st Named Inventor: Mark T. Bohr Express Mail No.: EV339917159US

Sheet: 1 of 4

Docket No.: 42P15335

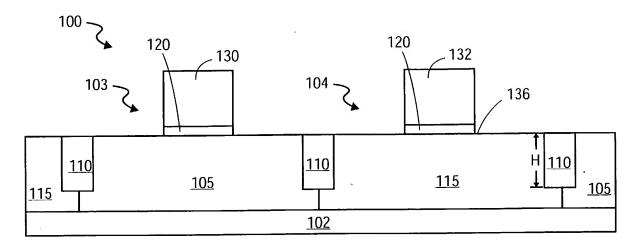


FIG. 1

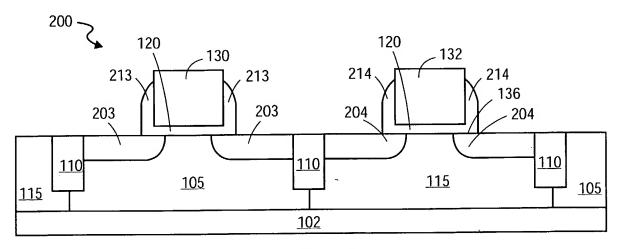


FIG. 2

Blakely, Sokoloff, Taylor & Zafman LLP (310) 207-3800 Title: PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED

JUNCTION REGIONS

1st Named Inventor: Mark T. Bohr Express Mail No.: EV339917159US

Sheet: 2 of 4

Docket No.: 42P15335

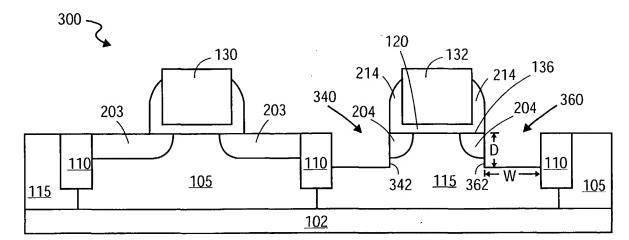


FIG. 3

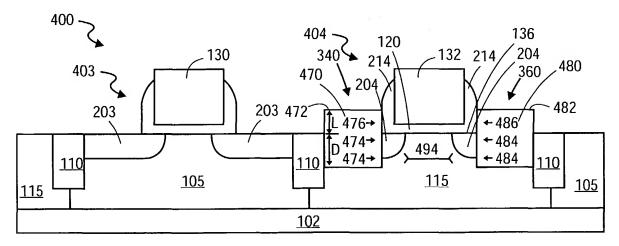


FIG. 4

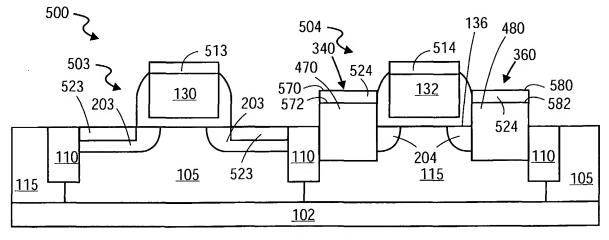


FIG. 5

Blakely, Sokoloff, Taylor & Zafman LLP (310) 207-3800 Title: PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED JUNCTION REGIONS

1st Named Inventor: Mark T. Bohr Express Mail No.: EV339917159US

Docket No.: 42P15335

Sheet: 3 of 4

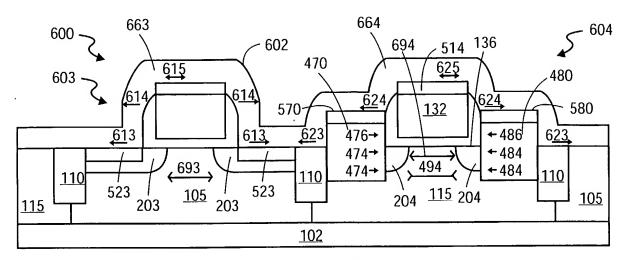


FIG. 6

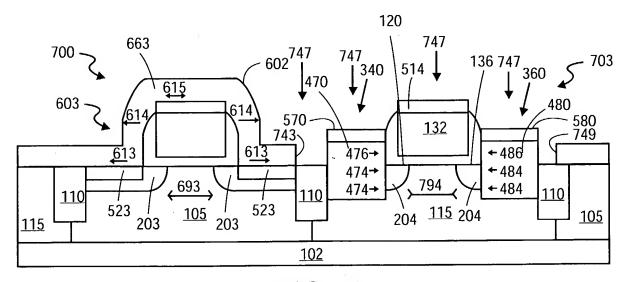


FIG. 7

Blakely, Sokoloff, Taylor & Zafman LLP (310) 207-3800

Title: PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED JUNCTION REGIONS

, 1st Named Inventor: Mark T. Bohr Express Mail No.: EV339917159US

Sheet: 4 of 4

Docket No.: 42P15335

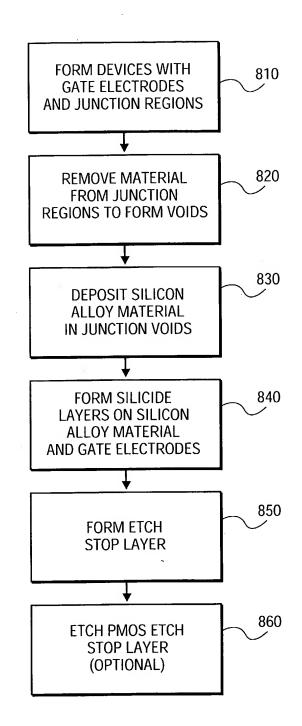


FIG. 8